



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,609	05/18/2004	William Wang	12790-US-PA	3608
31561 7590 08/02/2007 JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE 7 FLOOR-1, NO. 100 ROOSEVELT ROAD, SECTION 2 TAIPEI, 100 TAIWAN			EXAMINER VIDWAN, JASJIT S	
			ART UNIT 2182	PAPER NUMBER
			NOTIFICATION DATE 08/02/2007	DELIVERY MODE ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USA@JCIPGROUP.COM.TW

<b>Office Action Summary</b>	<b>Application No.</b> 10/709,609	<b>Applicant(s)</b> WANG, WILLIAM	
	<b>Examiner</b> Jasjit S. Vidwan	<b>Art Unit</b> 2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 17 May 2007.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

**DETAILED ACTION**

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pattisam et al, U.S. Patent No: 5,357,614 [herein after **Pattisam**] and further in view of Karpoff et al U.S. Patent No: 6,857,059 [herein after **Karpoff**].

1. As per Claim 1, Pattisam teaches a data compression/decompression device [see Fig. 3, element 20, "**Data compression controller**"], suitable for compressing/decompressing [see Col. 2, Lines 48-52 – the 'Data compression controller' decompresses data as well] a data transmitted between a data generation device [see Fig. 3, element 200, "**Host or I/O channel**"] and a data storage device [see Fig. 3, element 280, "**SCSI Devices**" – Also Col. 2, Lines 27-29 – SCSI Device could be storage device], comprising:

- (a) Input buffer [see Fig. 3, elements 210 & 211], for buffering and storing said data for input [see Col. 11, Lines 58-60]
- (b) Output buffer [see Fig. 3, elements 250], for buffering and storing said data for output [see Col. 12, Lines 35-36]
- (c) Data compressor/decompressor [see Fig. 3, elements 220, "**Data compression coprocessor**"], coupled to said output buffer [Fig. 3, elements 213 – Output data buffer is coupled to data compression coprocessor through compressed data bus 213], for

compressing/decompressing said data for input and storing said data for output in said output buffer [see Col. 2, Lines 50-52]

(d) Controller [see Fig. 3, element 230, "Microprocessor"], coupled to said input buffer, said output buffer and said data compressor/decompressor, for controlling data transmission with said data generation device and said data storage device controlling compressing/decompressing said data [Col. 8, Lines 44-58, *Microprocessor employs Data Comp coprocessor interface logic to control compression coprocessor*]

Pattisam teaches the above limitations in addition to teaching a system wherein the microprocessor issues starting and ending addresses to SCSI interface logic for the data located in the data buffer (compressed data from host) [see Col. 15, Lines 41-45]. Pattisam goes further to disclose a system wherein the SCSI controller interface logic after receiving the starting and ending addresses from the microprocessor further identifies the addresses of the said data to the SCSI controller which is written to external device (storage devices) [Col. 12, Line 63 – Col. 13, Line 1]. Therefore, it follows that Pattisam teaches a microprocessor, which manages data addresses, issued by the host with that of physical address of storing the data in said data storage device (via use of SCSI interface logic and SCSI controller). However despite the above teachings, Pattisam fails to expressly teach performing the above function by way of "address mapping table" which is the cross reference between an access address transmitted from data generation device and physical address of storing the data in said data storage device.

Karpoff teaches the above deficiency by teaching a system wherein the microprocessor manages the mapping table which is the cross reference between an access address transmitted from data generation device (host) and a physical address of storing the data in data storage device [see Karpoff, Col. 4, Lines 23-36]. It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the two teachings in order to take advantage of having a system where the host application never has to deal with volume resizing and spare capacity can be amortized across multiple disk images, thus lowering the cost associated with "on reserve" storage capacity [see Karpoff, Col. 3, Lines 46-64]

2. **As per Claim 5**, Pattisam as modified by Karpoff above teaches a data compression/decompression device, comprising:

- (a) Data storage device [see Fig. 3, element 280, "*SCSI Devices*" – Also Col. 2, Lines 27-29 – *SCSI Device could be storage device*] having a data transmission interface [Fig. 3, elements 260 & 270 – "*SCSI controller Interface Logic*" & "*SCSI controller*"]
- (b) Data generation device [see Fig. 3, element 200, "*Host or I/O channel*"], accessing a data in said data storage device via said data transmission interface [see Col. 2, Lines 48-52]; and a data compression/decompression device coupled to said data storage device and said data generation device via said data transmission interface [see Fig. 3, element 20, "*Data compression controller*"], for compressing/decompressing said data transmitted between said data storage device and said data generation device [Col. 4, Lines 17-24] and managing an address mapping table which is the cross reference between an access address transmitted from said data generation and a physical address of storing said data storage device [see Karpoff, Col. 4, Lines 23-36]

3. **As per Claim 2 and 7**, Pattisam as modified by Karpoff above teaches a device wherein said controller includes:

- (a) Data generation control unit [see Fig. 3, element 215, "*Command/Data Registers Application Interface Logic*"], for controlling data transmission with said data generation device
- (b) Data storage control unit [Fig. 3, element 260, "*SCSI controller Interface Logic*"], for controlling data transmission with said data storage device
- (c) Data extractor, for obtaining said data from said input buffer, extracting a compressing/decompressing portion of said data, and sending said compression/decompression portion of said data to said data compressor / decompressor [Fig. 3, element 216, "*Data Comp coprocessor Interface Logic*"]

(d) Main control unit for coordinating and controlling said data generation control unit, said data storage control unit, and said data extractor, and for managing said address mapping [Fig. 3, element 230, "Microprocessor"]

4. As per Claim 3 and 8, Pattisam as modified by Karpoff above teaches a device wherein said data generation device is at least one of a host, a laptop computer, a microprocessor, an interface card and a router [see Fig. 3, element 200, "Host or I/O channel"]

5. As per Claim 4 and 9, Pattisam as modified by Karpoff above teaches a device wherein said data storage device is at least one of a hard disk drive, floppy disk drive, a CD-RW drive, a magnetic-optical device, a digital video recorder and a flash memory card [see Col. 4, Lines 5-9, "...SCSI compatible device specifically a tape drive, for storage of data in a compressed format"]

6. As per Claim 6, see rejection of Claim 1 above

#### **Response to Arguments**

7. Applicant's arguments filed 5/17/07 have been fully considered but they are not persuasive.

Applicant argues:

(a) Primary prior art of record (Pattisam) fails to teach the "address-mapping table" and though secondary reference teaches the deficiency, Pattisam and Karpoff are not combinable since both inventions are mutually exclusive.

8. With respect to argument (a), **Examiner disagrees**. Applicant argues that Primary reference (Pattisam) does not teach "address-mapping table" used for cross reference and in fact uses Microprocessor (230) which issues starting and ending addresses to SCSI interface logic and wherein the SCSI controller interface logic (260) further identifies the starting and ending addresses to SCSI controller. Therefore, contrary to the cross-reference address-mapping table being used by present application for providing the starting/ending addresses, it is the SCSI controller that issues the addresses under prior art. However, Applicant goes on to agree that Karpoff et al does disclose the above limitation of providing an address-mapping table to handle address distribution. However, Applicant submits his position that since Pattisam is geared towards having the Microprocessor/SCSI controller be responsible

for data addressing, the above two references are not combinable since both inventions are mutually exclusive to reach different solutions to a problem. It should be noted that the Examiner is relying on the combination of Karpoff's address mapping table to be substituted into the Pattisam in order to relieve the microprocessor and SCSI controller from the duties of providing the starting and ending addresses thereby allowing the said processors in focusing on other aspects of operation. Therefore as should be obvious to one of ordinary skill in the art, the combination of the two references would thereby render Pattisam's usage of microprocessor for providing starting/ending address and thereby passing over the duties to the use of cross reference address table for data address distribution. A sufficient above stated motivation was provided in the original office action and therefore it is the position of the Examiner that prior art as combined still reads on the current limitations of present invention.

***Conclusion***

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasjit S. Vidwan whose telephone number is (571) 272-7936. The examiner can normally be reached on 8am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, KIM HUYNH can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2182

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JSV  
7/23/07



KIM HUYNH  
SUPERVISORY PATENT EXAMINER  
7/25/07